FIG. 1

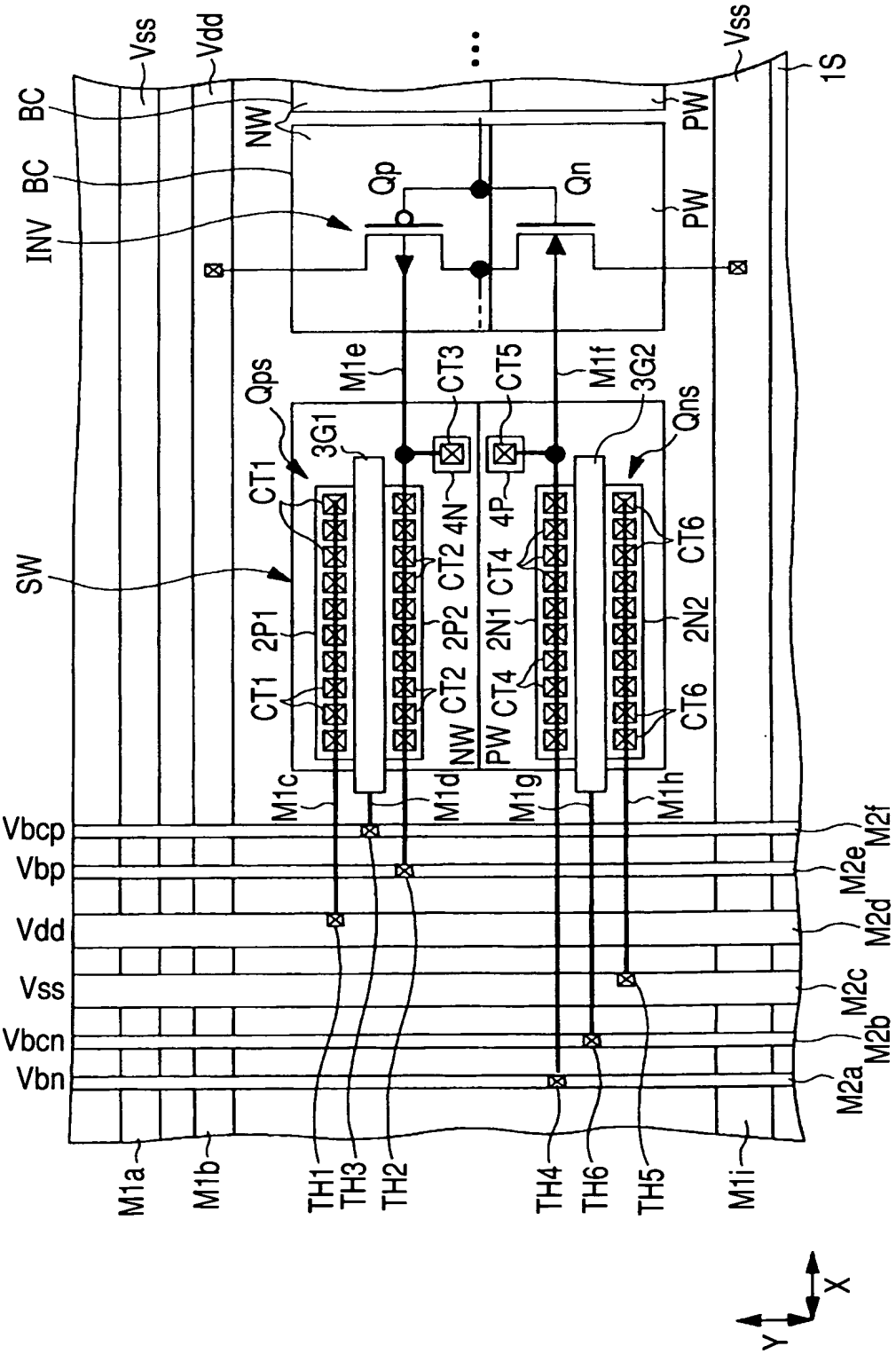

Vss
Vdd
Vss
1S
BC
BC
INV
NW
PW
PW
Qp
Qn
SW
Qps
Qns
M1e
M1f
CT3
CT5
3G1
3G2
CT1
4N
4P
CT6
CT2
2P1
2P2
2N1
2N2
CT4
NW
PW
M1c
M1d
M1g
M1h
Vbcp
Vbp
Vdd
Vss
Vbcn
Vbn
M2f
M2e
M2d
M2c
M2b
M2a
M1a
M1b
TH1
TH3
TH2
TH4
TH6
TH5
M1i
X
Y

FIG. 2

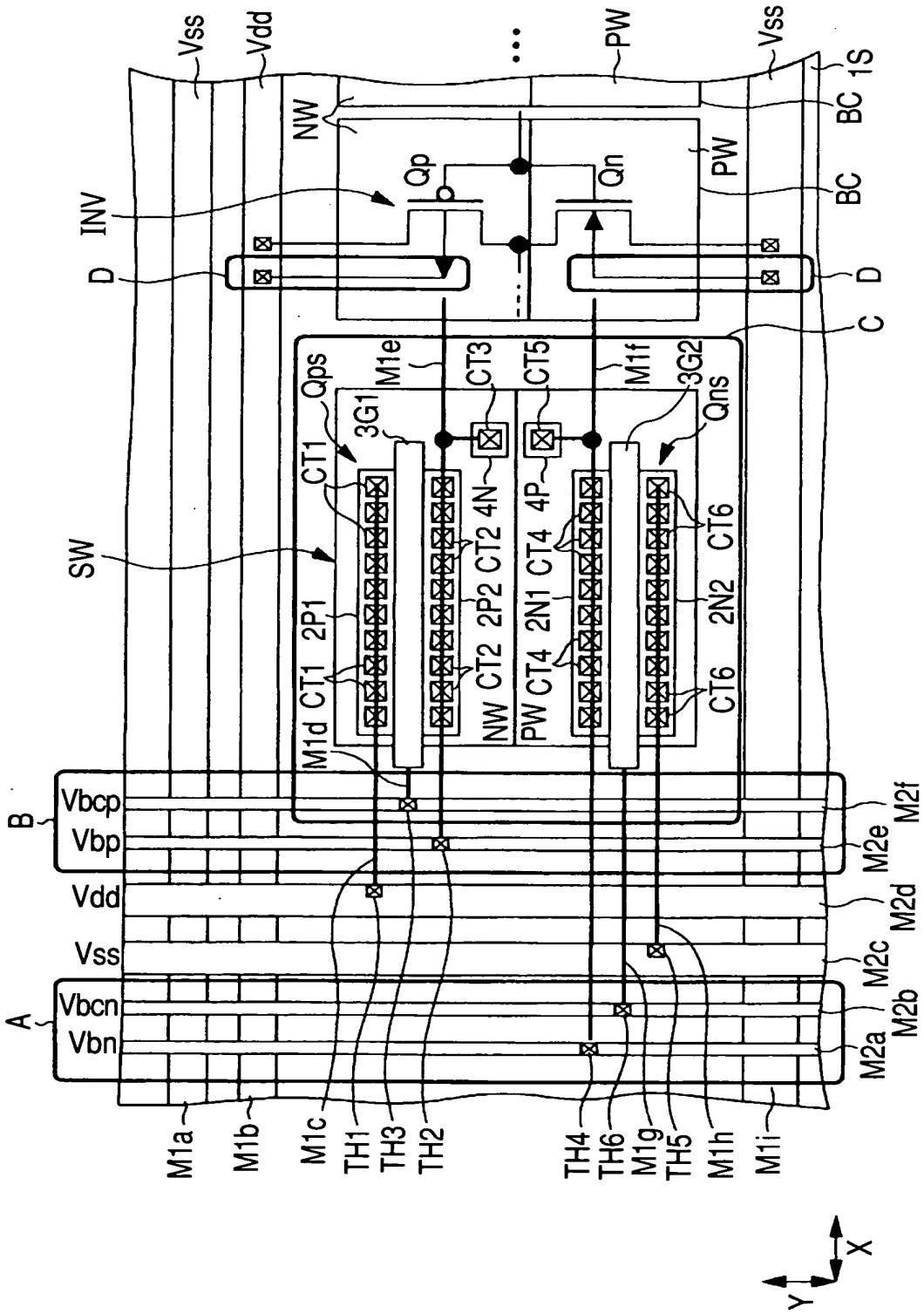
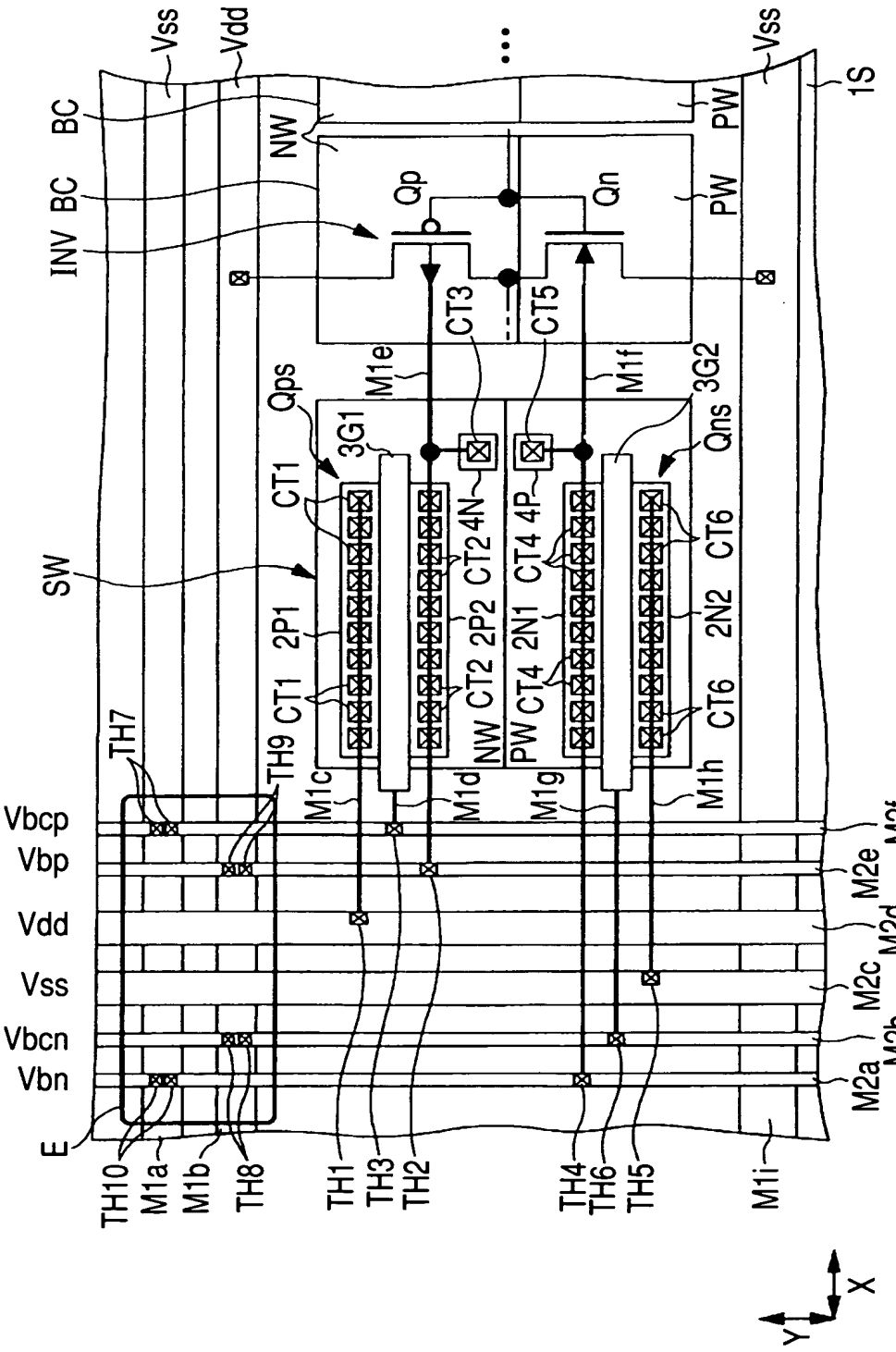

Vss
Vdd
PW
Vss
BC 1S
NW
PW
BC
Qp
Qn
INV
D
D
C
Qps
M1e
CT3
CT5
M1f
3G2
Qns
3G1
CT1
SW
4N
4P
CT6
2P1
2P2
CT2
2N1
CT4
2N2
CT6
M1d CT1
CT2
NW
CT2
PW
CT4
CT6
B
Vbcp
Vbp
Vdd
Vss
A
Vbcn
Vbn
M2f
M2e
M2d
M2c
M2b
M2a
M1a
M1b
M1c
TH1
TH3
TH2
TH4
TH6
M1g
TH5
M1h
M1i
X
Y

FIG. 3



1S : SEMICONDUCTOR SUBSTRATE
SW : SLAVE SWITCH CIRCUIT CELL
BC : CIRCUIT CELL

M1a,M1i : WIRING (FIRST WIRING)
M2b,M2f : WIRING (SECOND WIRING)
M2a,M2e : WIRING (THIRD WIRING)

FIG. 4

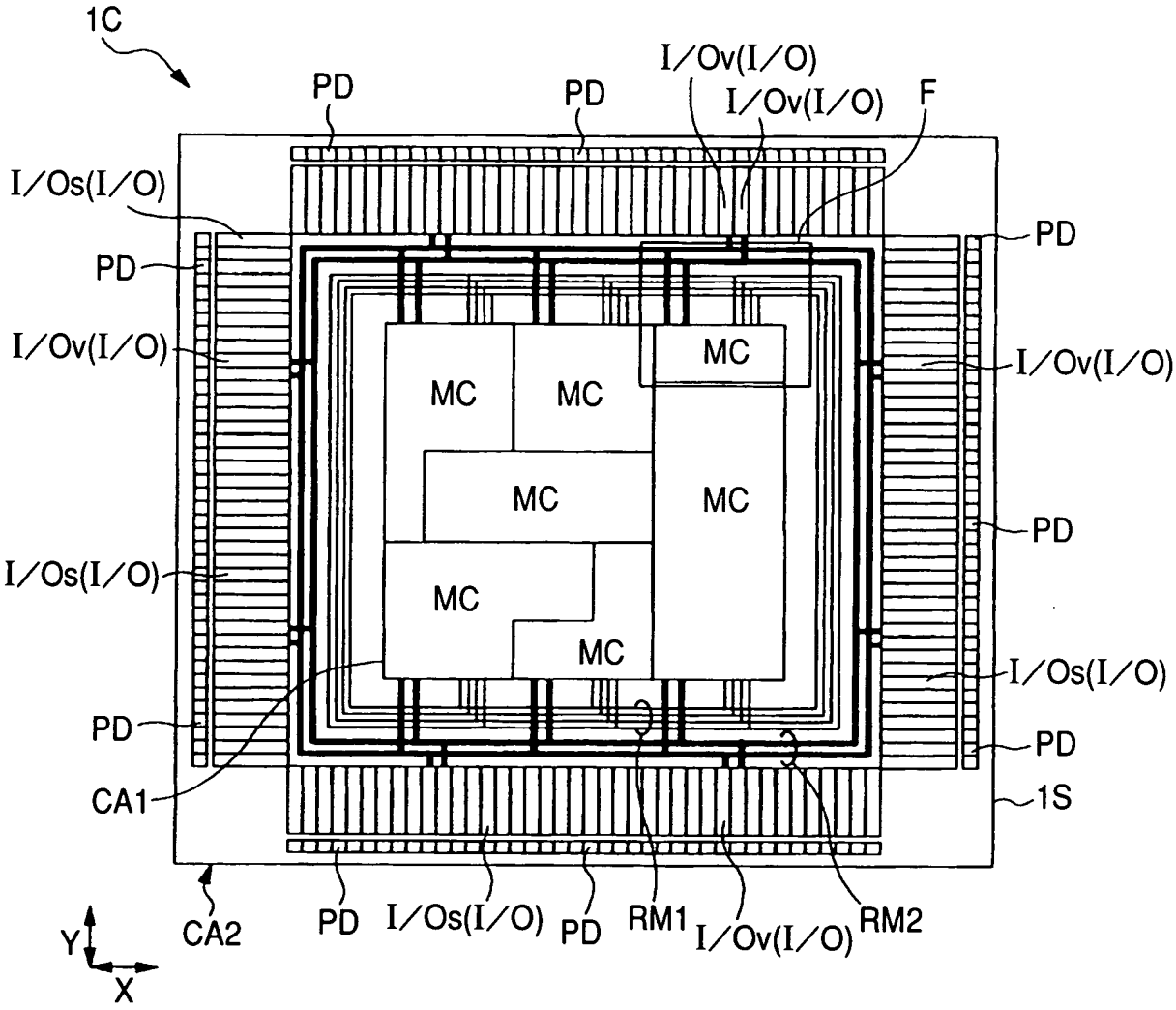

1C
PD
PD
I/Ov(I/O)
I/Ov(I/O)
F
I/Os(I/O)
PD
I/Ov(I/O)
MC
MC
MC
MC
MC
MC
MC
I/Os(I/O)
PD
CA1
PD
I/Ov(I/O)
PD
I/Os(I/O)
PD
I/Os(I/O)
PD
1S
CA2
PD
I/Os(I/O)
PD
RM1
I/Ov(I/O)
RM2
Y
X

FIG. 5

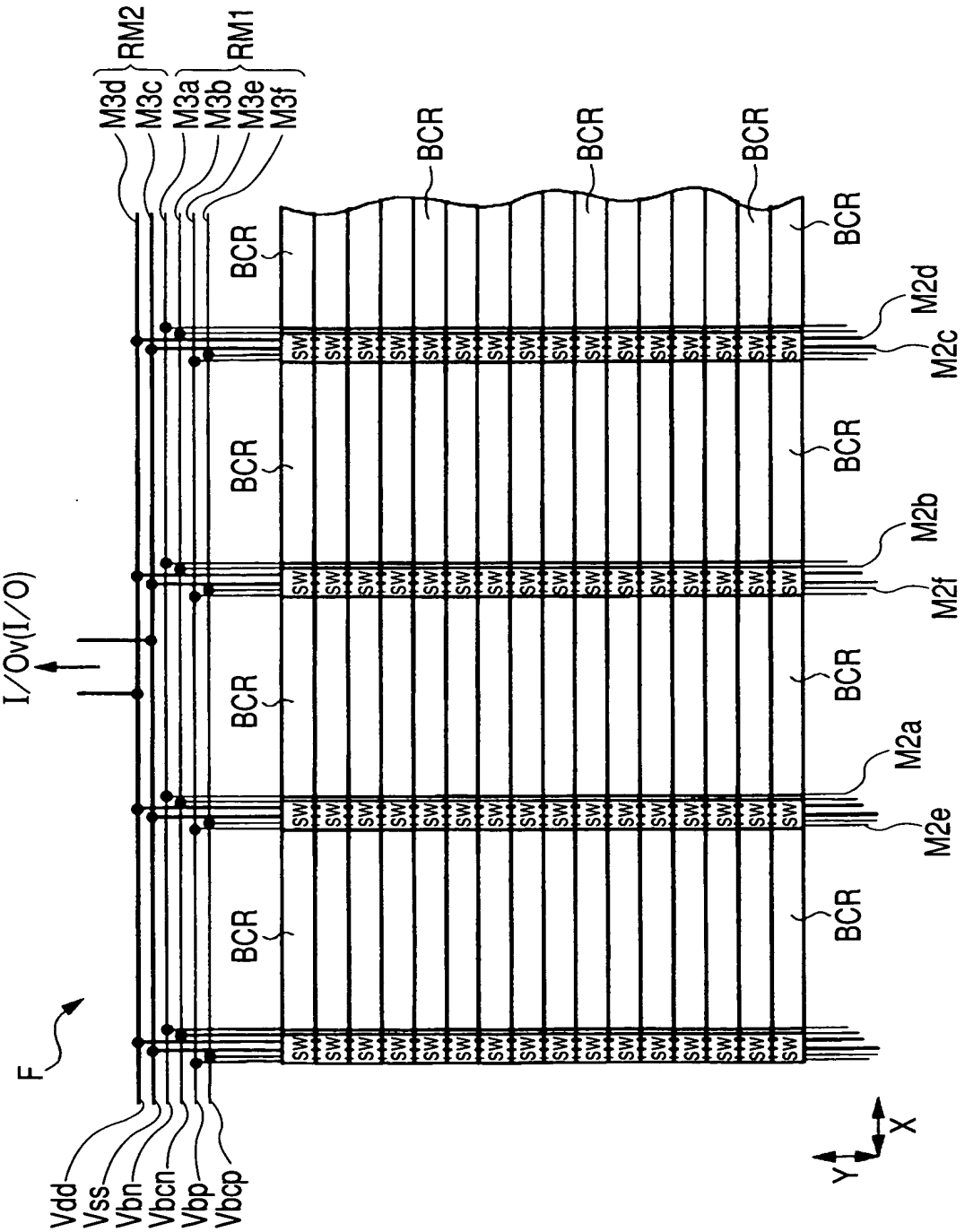

RM2
RM1
M3d
M3c
M3a
M3b
M3e
M3f
BCR
SW
M2d
M2c
M2b
M2f
M2a
M2e
I/Ov(I/O)
F
Vdd
Vss
Vbn
Vbcn
Vbp
Vbcp
X
Y

FIG. 6

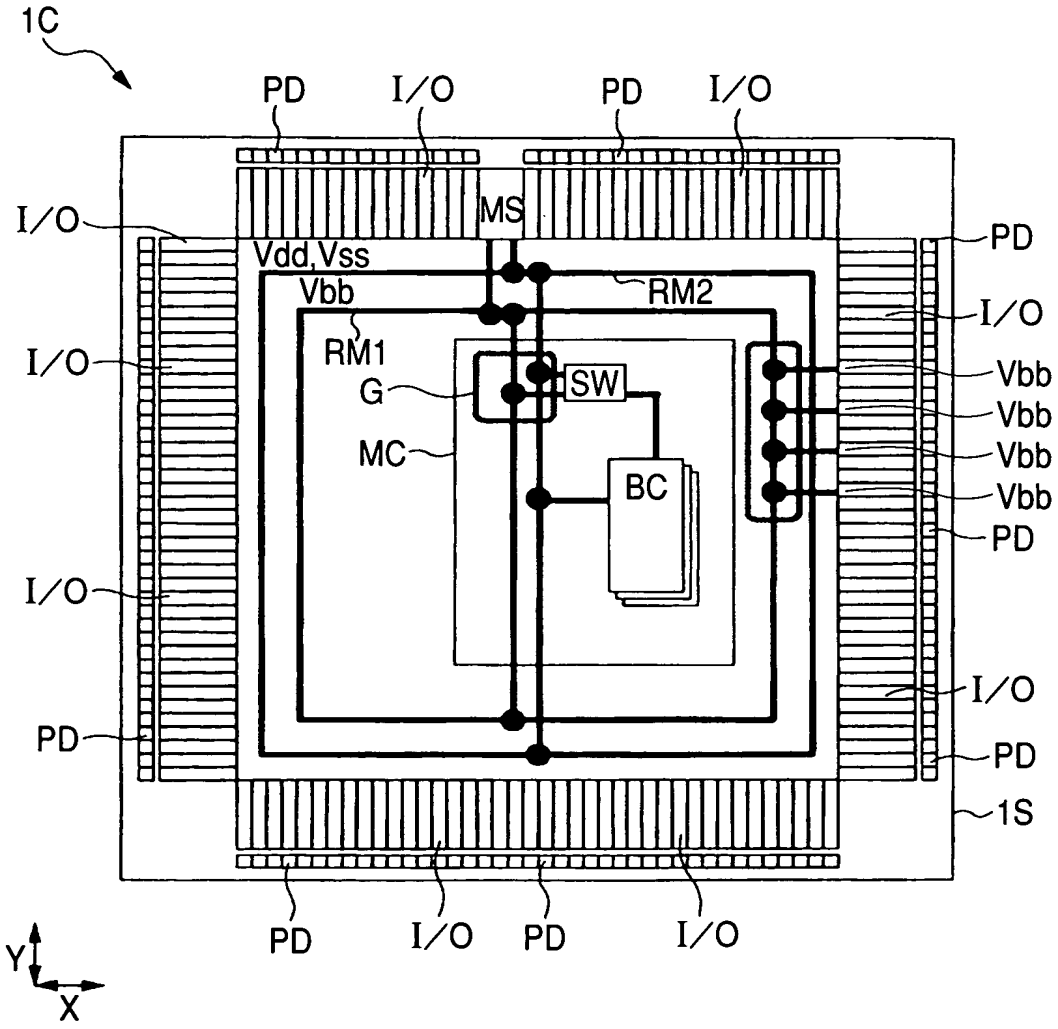

1C
PD
I/O
PD
I/O
I/O
MS
Vdd,Vss
Vbb
RM2
RM1
G
SW
MC
BC
PD
I/O
Vbb
Vbb
Vbb
Vbb
PD
I/O
PD
I/O
PD
1S
PD
I/O
PD
I/O
Y
X

FIG. 7

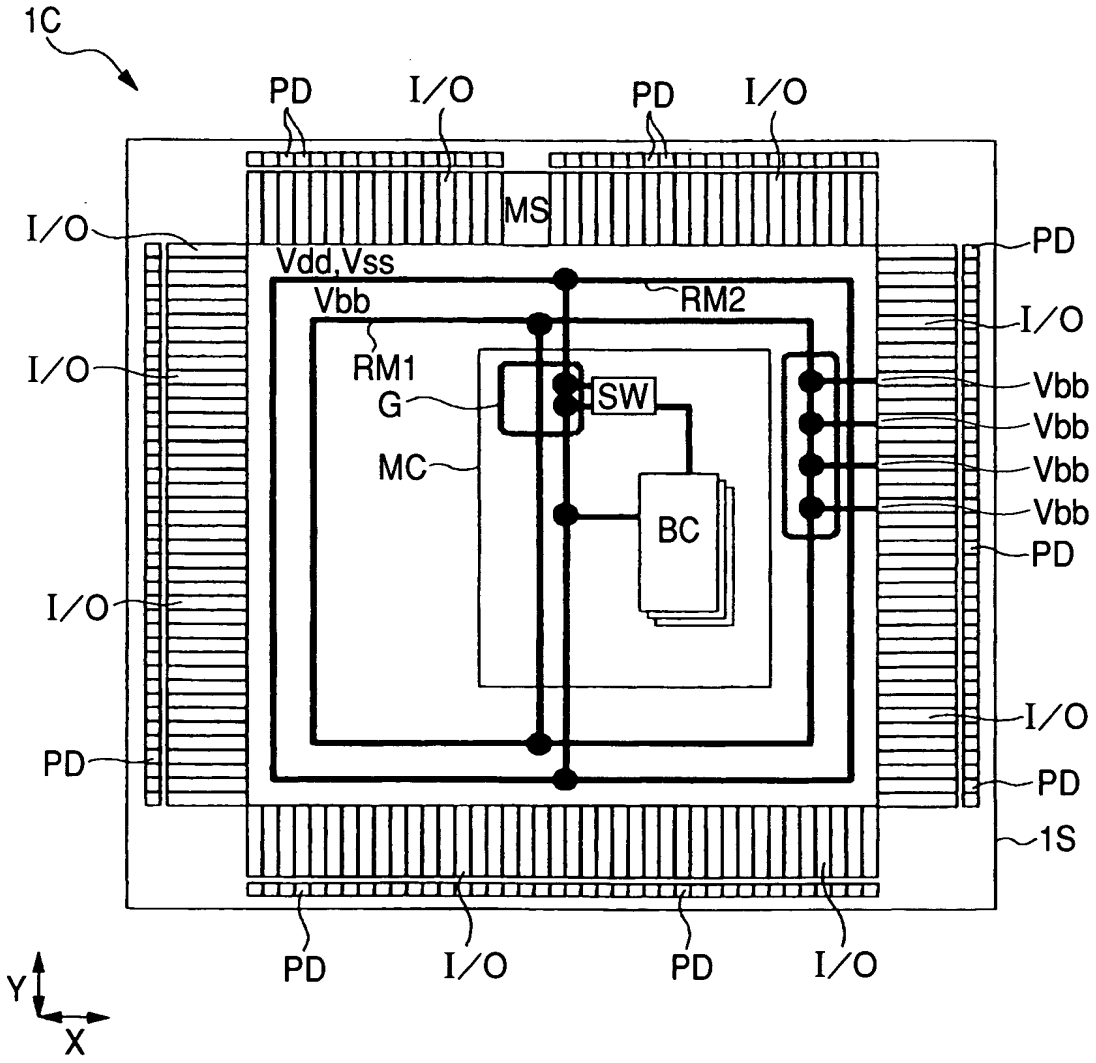

1C
PD
I/O
PD
I/O
MS
I/O
Vdd,Vss
Vbb
RM2
RM1
G
SW
MC
BC
I/O
I/O
PD
Vbb
Vbb
Vbb
Vbb
PD
I/O
PD
1S
PD
I/O
PD
I/O
Y
X

FIG. 8

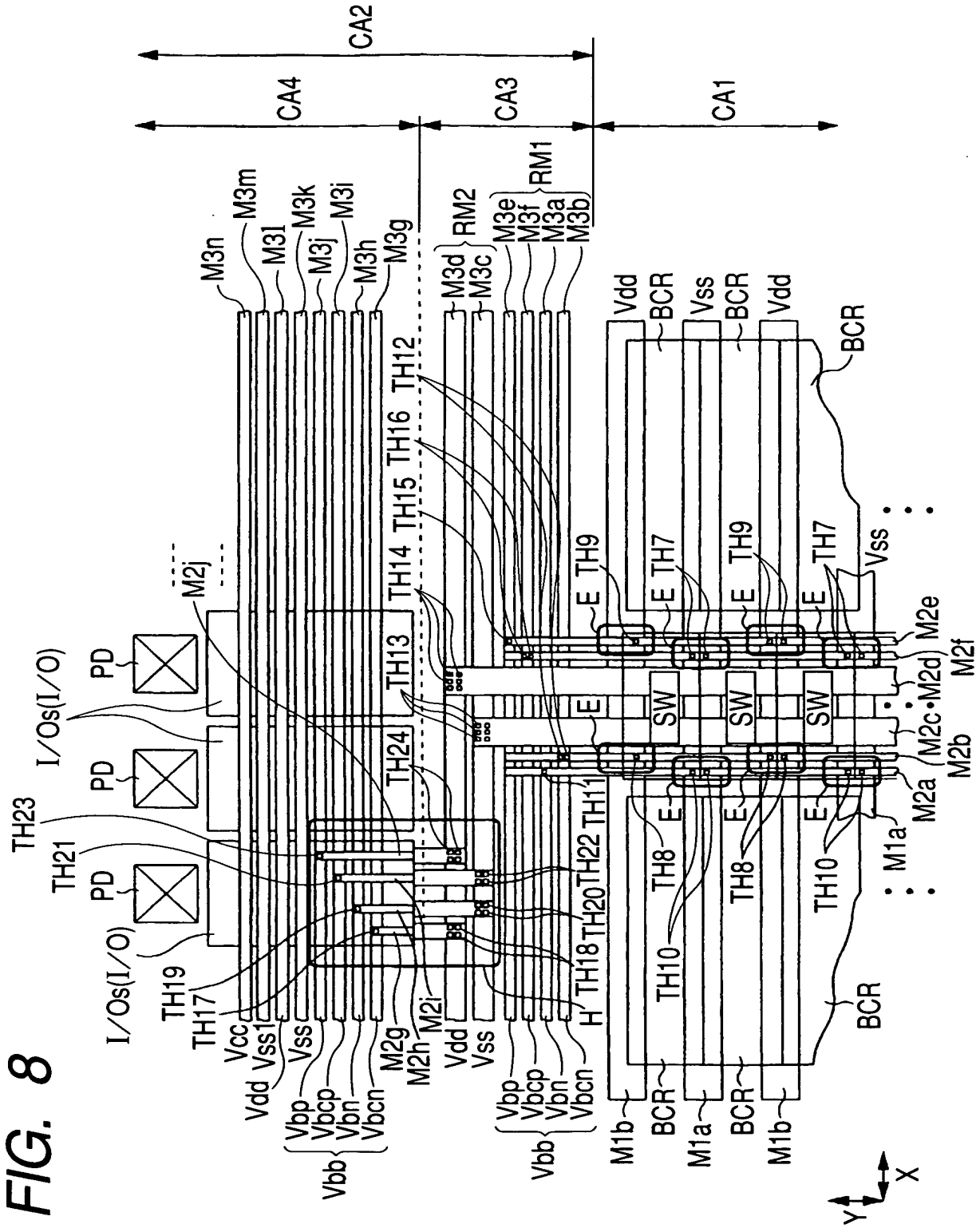

CA2
CA4
CA3
CA1
M3n
M3m
M3l
M3k
M3j
M3i
M3h
M3g
M3d
M3c
RM2
M3e
M3f
M3a
M3b
RM1
M2j
I/Os(I/O)
PD
TH23
TH21
TH19
TH17
TH12
TH16
TH15
TH14
TH13
TH24
Vcc
Vss1
Vdd
Vss
Vbp
Vbcp
Vbn
Vbcn
Vbb
M2g
M2h
M2i
TH18
TH20
TH22
TH11
E
TH9
TH7
SW
TH8
TH10
BCR
M1b
M1a
M2a
M2b
M2c
M2d
M2e
M2f
X
Y

FIG. 9

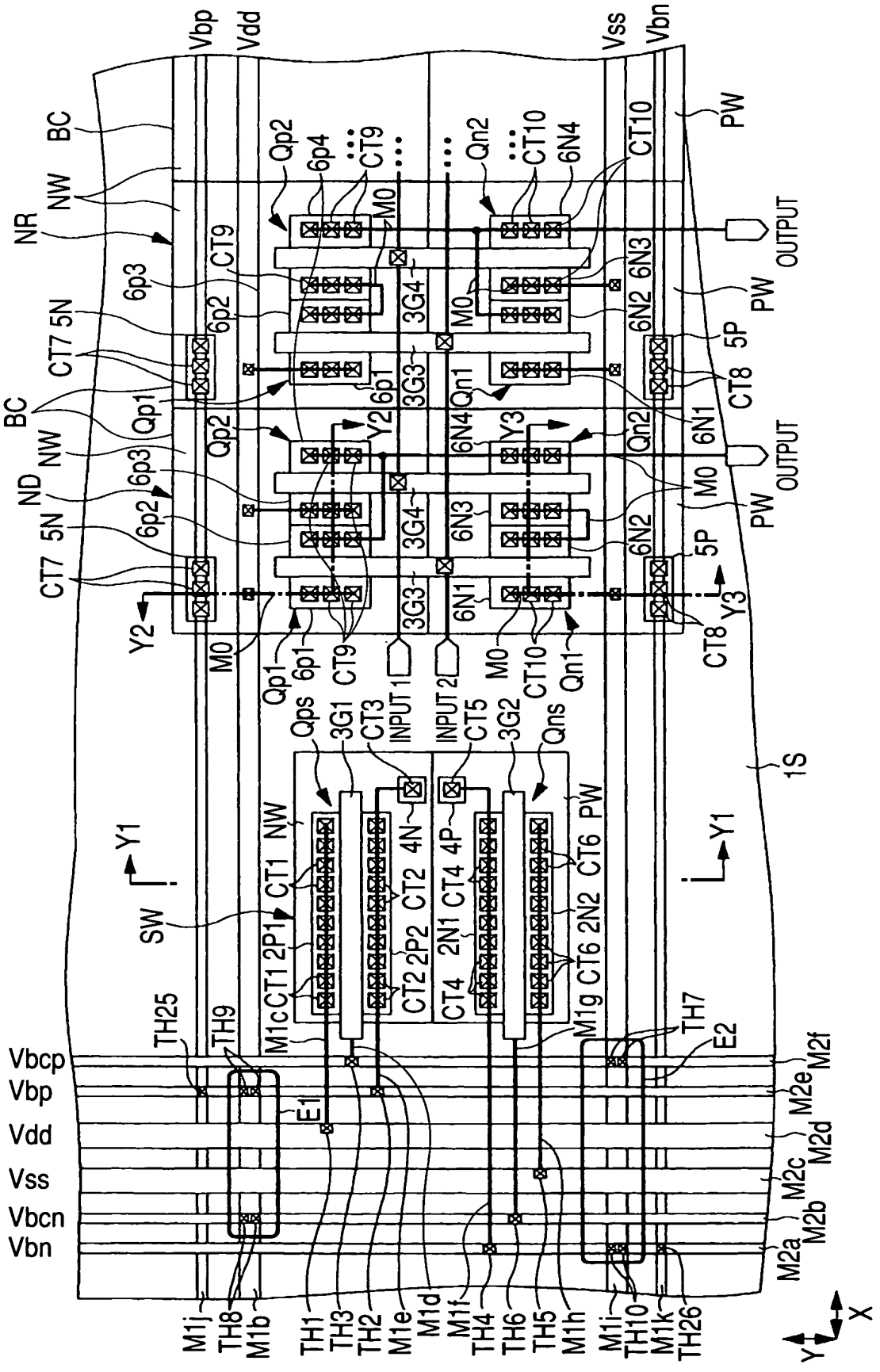

Vbp
Vdd
Vss
Vbn
BC
NW
NR
ND
PW
OUTPUT
Qp1
Qp2
Qn1
Qn2
Qps
Qns
6p1
6p2
6p3
6p4
6N1
6N2
6N3
6N4
5P
5N
3G1
3G2
3G3
3G4
4P
4N
2P1
2P2
2N1
2N2
CT1
CT2
CT3
CT4
CT5
CT6
CT7
CT8
CT9
CT10
M0
INPUT 1
INPUT 2
Y1
Y2
Y3
SW
1S
TH1
TH2
TH3
TH4
TH5
TH6
TH7
TH8
TH9
TH10
TH25
TH26
E1
E2
M1b
M1c
M1d
M1e
M1f
M1g
M1h
M1i
M1j
M1k
M2a
M2b
M2c
M2d
M2e
M2f
Vbcp
Vbcn
X
Y

FIG. 10

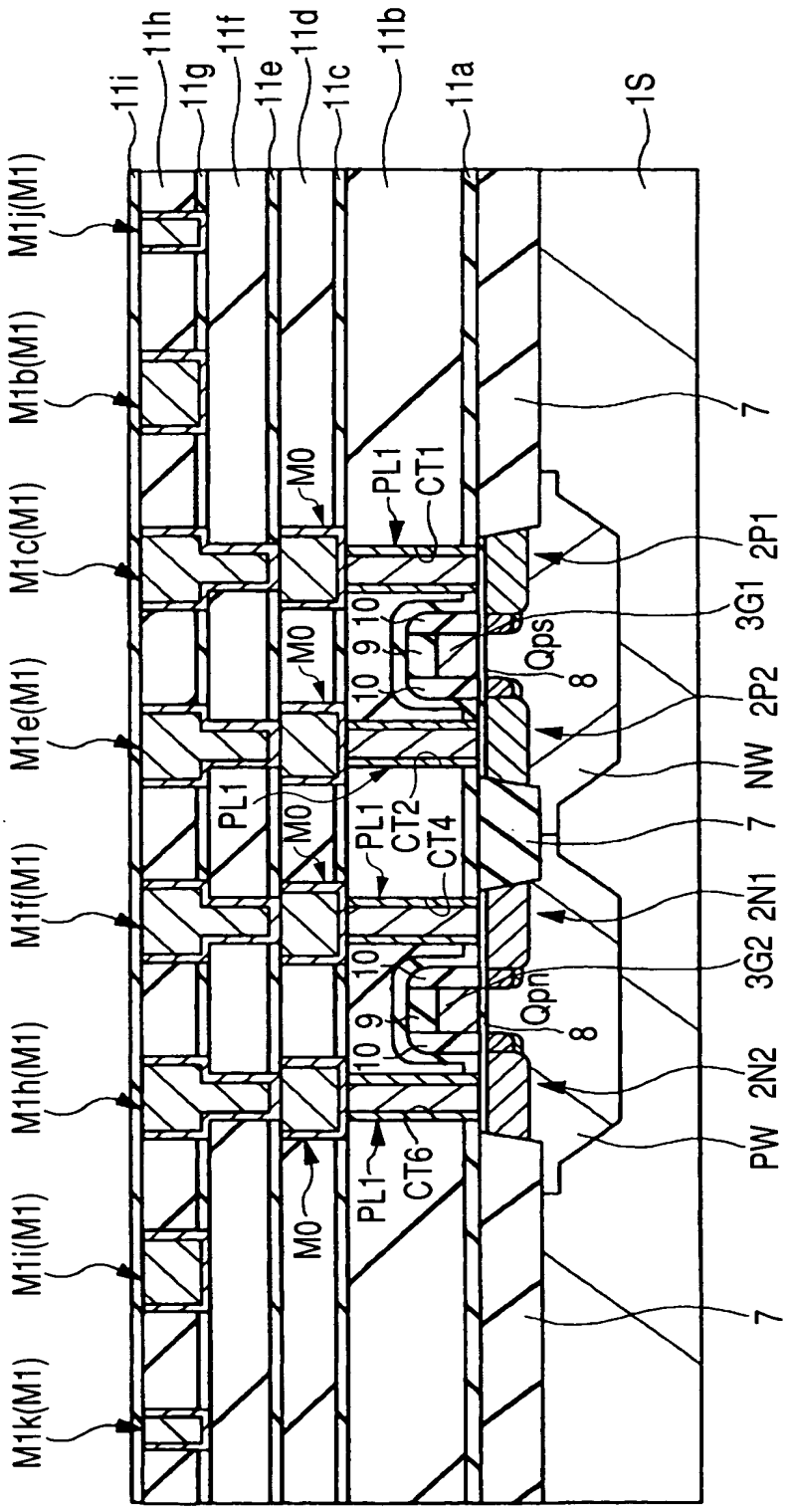

11i
11h
11g
11f
11e
11d
11c
11b
11a
1S
M1j(M1)
M1b(M1)
M1c(M1)
M1e(M1)
M1f(M1)
M1h(M1)
M1i(M1)
M1k(M1)
M0
PL1
CT1
CT2
CT4
CT6
10
9
Qps
Qpn
8
7
2P1
3G1
2P2
NW
2N1
3G2
2N2
PW

FIG. 11

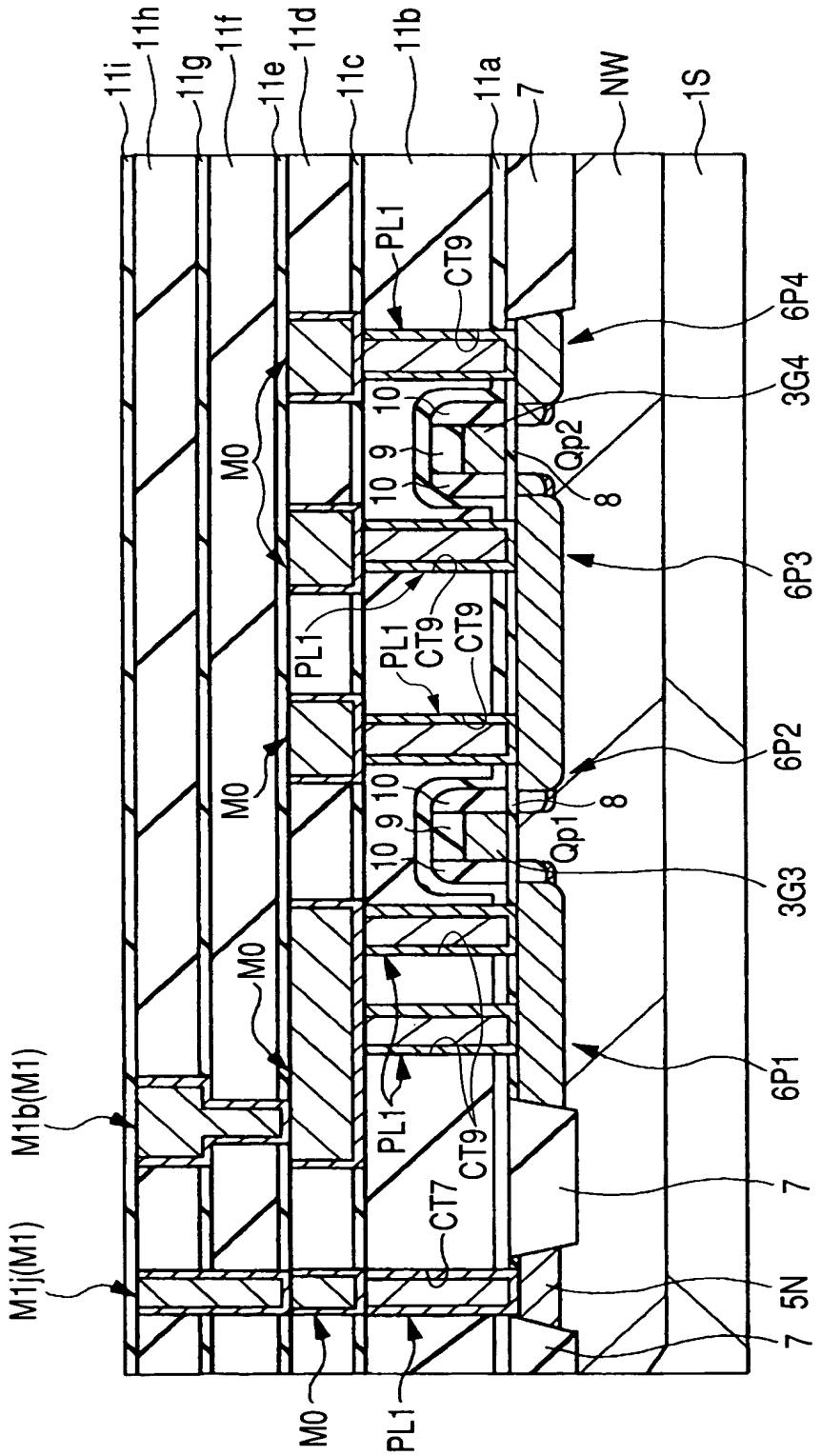

11i
11h
11g
11f
11e
11d
11c
11b
11a
7
NW
1S
PL1
CT9
6P4
3G4
10
9
Qp2
8
6P3
M0
6P2
Qp1
3G3
6P1
CT7
5N
M1b(M1)
M1j(M1)

FIG. 12

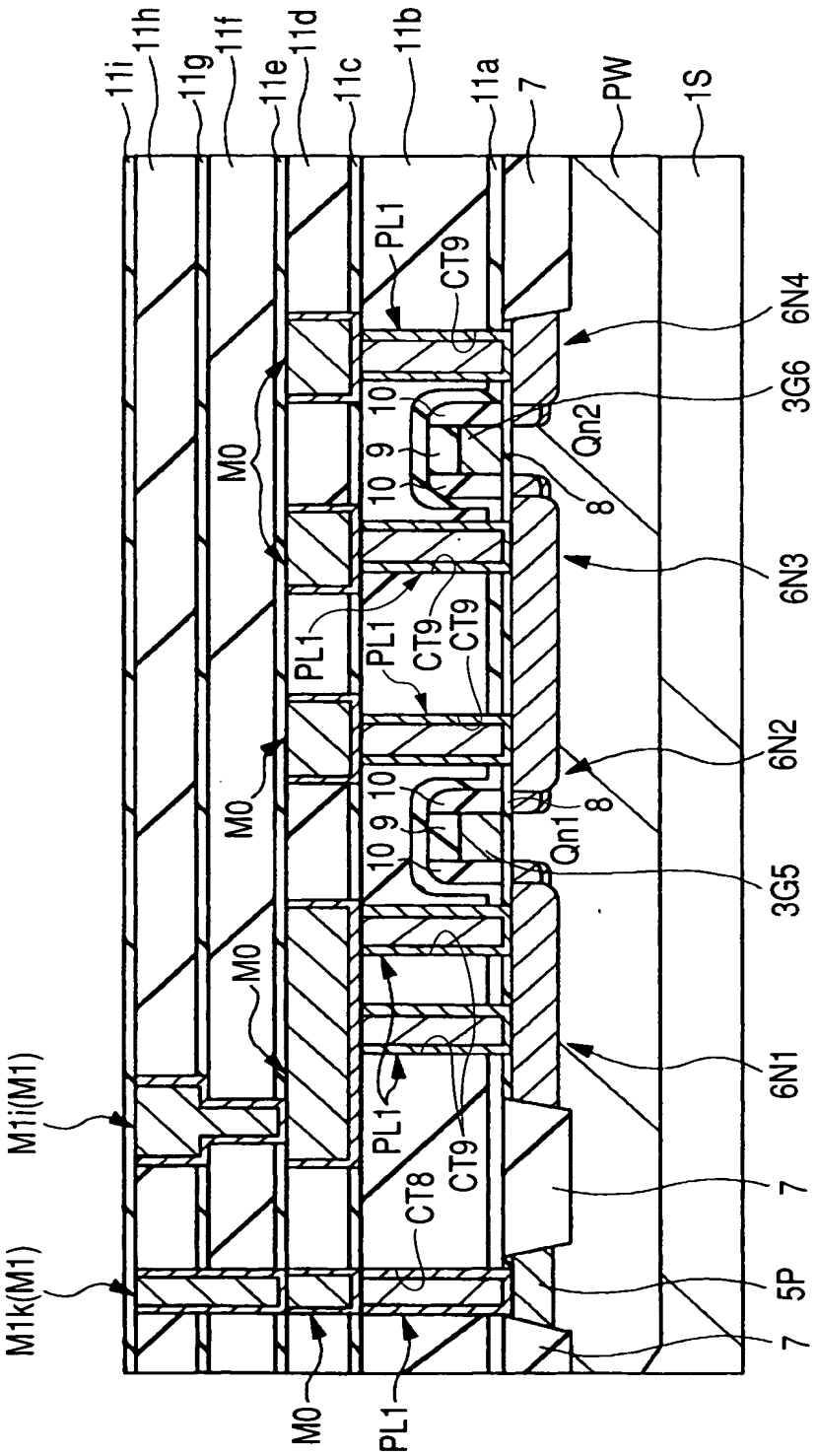

11i
11h
11g
11f
11e
11d
11c
11b
11a
7
PW
1S
PL1
CT9
6N4
3G6
10
9
Qn2
8
6N3
M0
CT9
6N2
Qn1
3G5
6N1
M1i(M1)
M1k(M1)
CT8
5P

FIG. 13

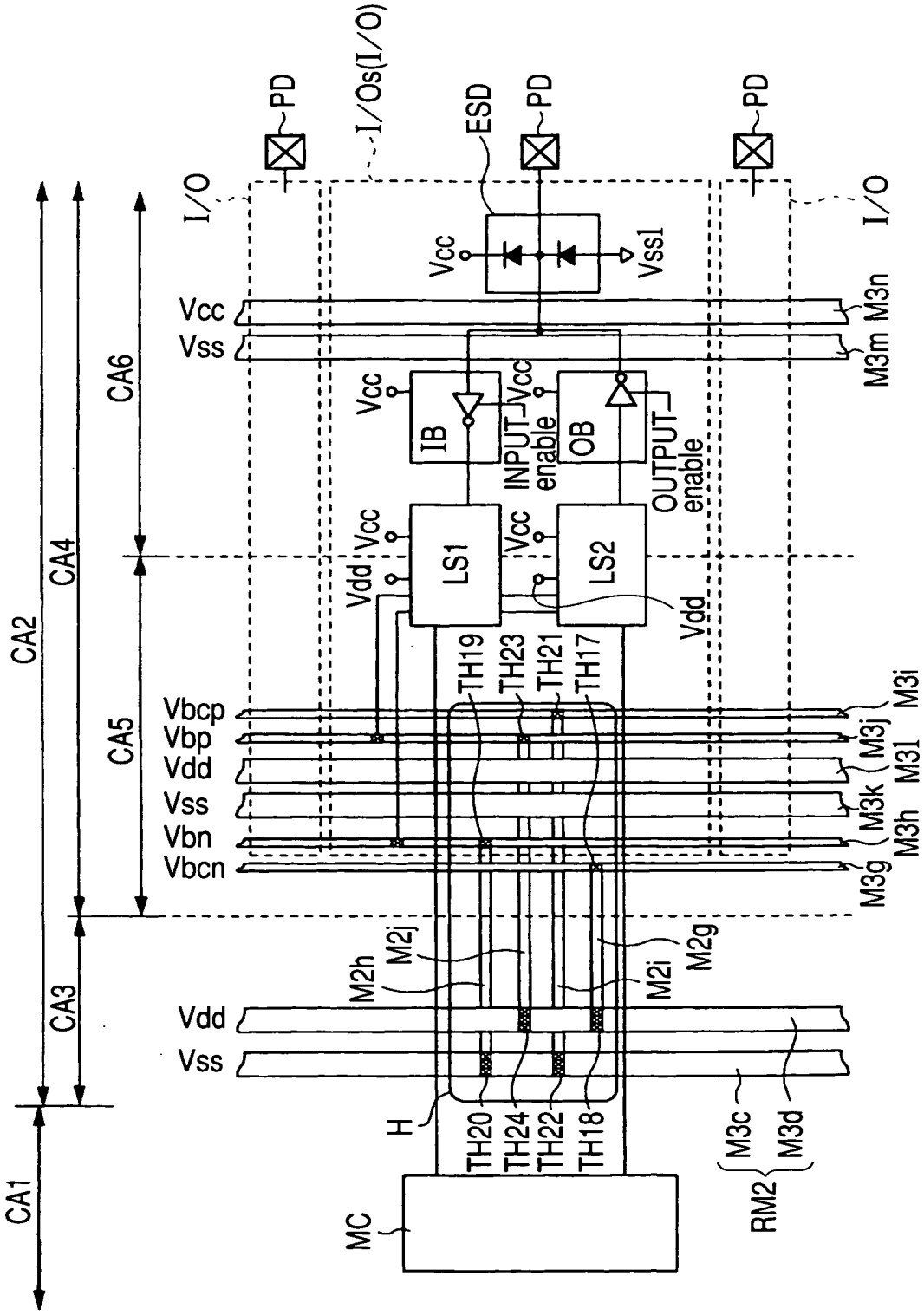

PD
I/Os(I/O)
ESD
PD
PD
I/O
I/O
Vcc
Vss1
Vcc
Vss
M3n
M3m
CA6
Vcc
IB
INPUT enable
Vcc
OB
OUTPUT enable
CA4
Vcc
Vdd
LS1
Vcc
LS2
Vdd
CA2
TH19
TH23
TH21
TH17
Vbcp
Vbp
Vdd
Vss
Vbn
Vbcn
CA5
M3i
M3j
M3l
M3k
M3h
M3g
M2h
M2j
M2i
M2g
CA3
Vdd
Vss
H
TH20
TH24
TH22
TH18
M3c
M3d
RM2
CA1
MC

FIG. 14

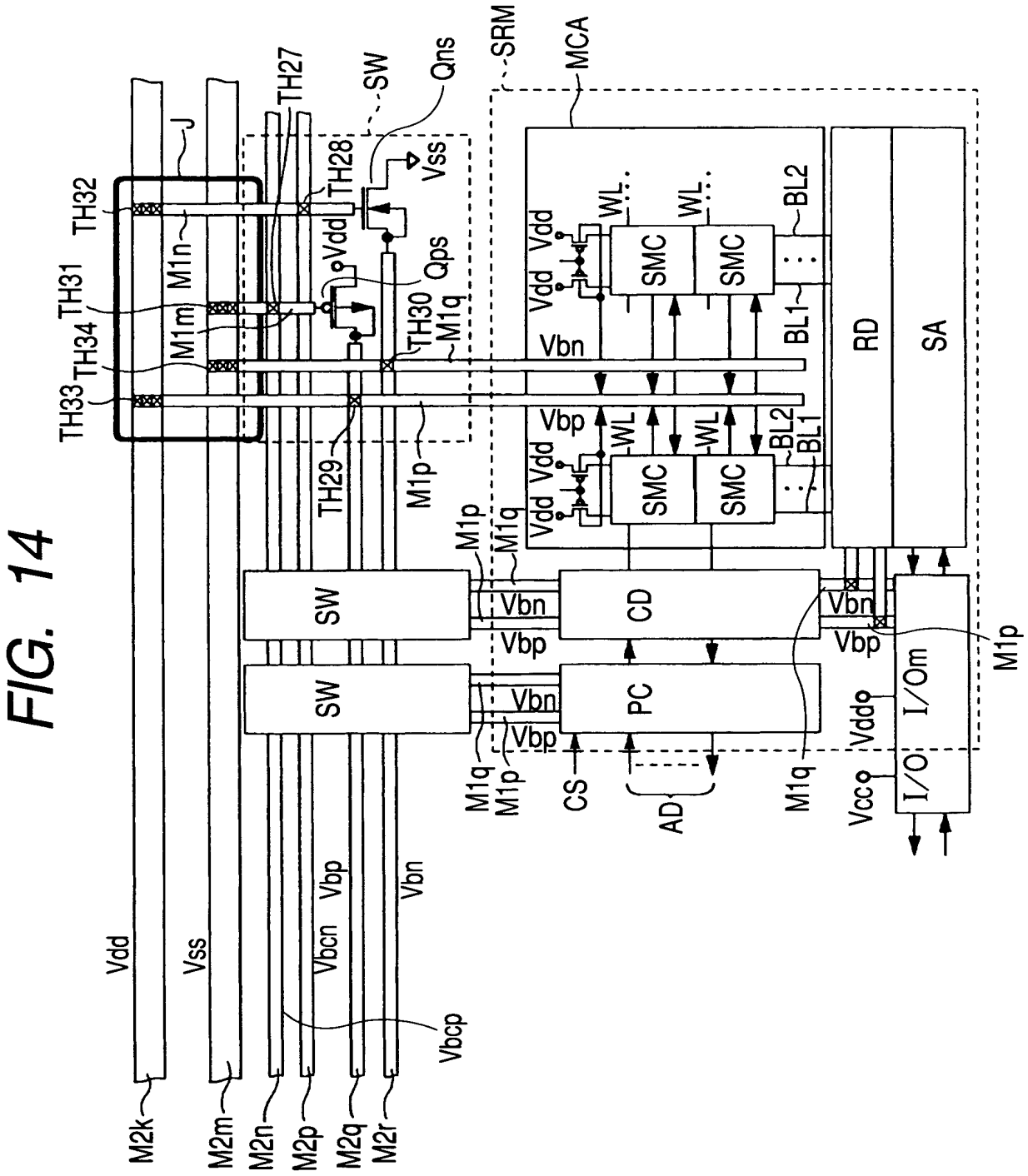

SRM
MCA
Qns
SW
TH27
TH28
Vss
Vdd
Qps
TH30
M1q
TH29
M1p
J
TH32
TH31
TH34
TH33
M1n
M1m
Vdd
Vss
Vbcn
Vbp
Vbn
Vbcp
M2k
M2m
M2n
M2p
M2q
M2r
SW
SW
CD
PC
Vbn
Vbp
M1q
M1p
CS
AD
WL
BL2
BL1
SMC
RD
SA
I/Om
I/O
Vcc

FIG. 15

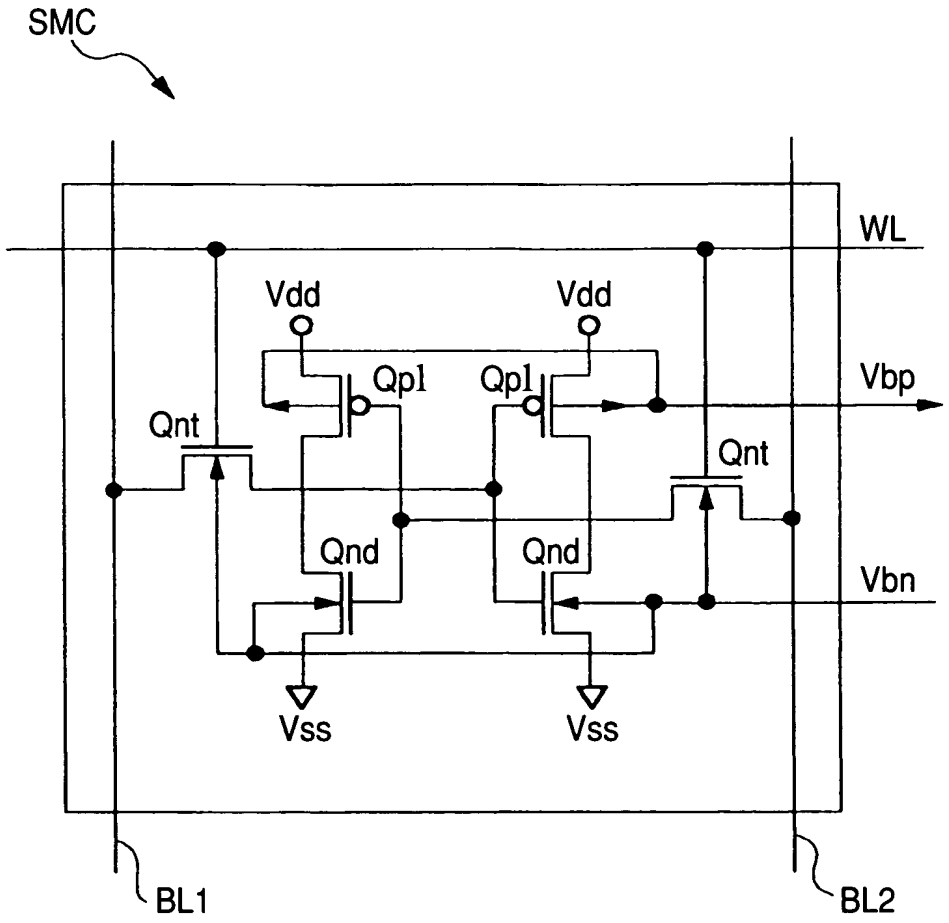


FIG. 16

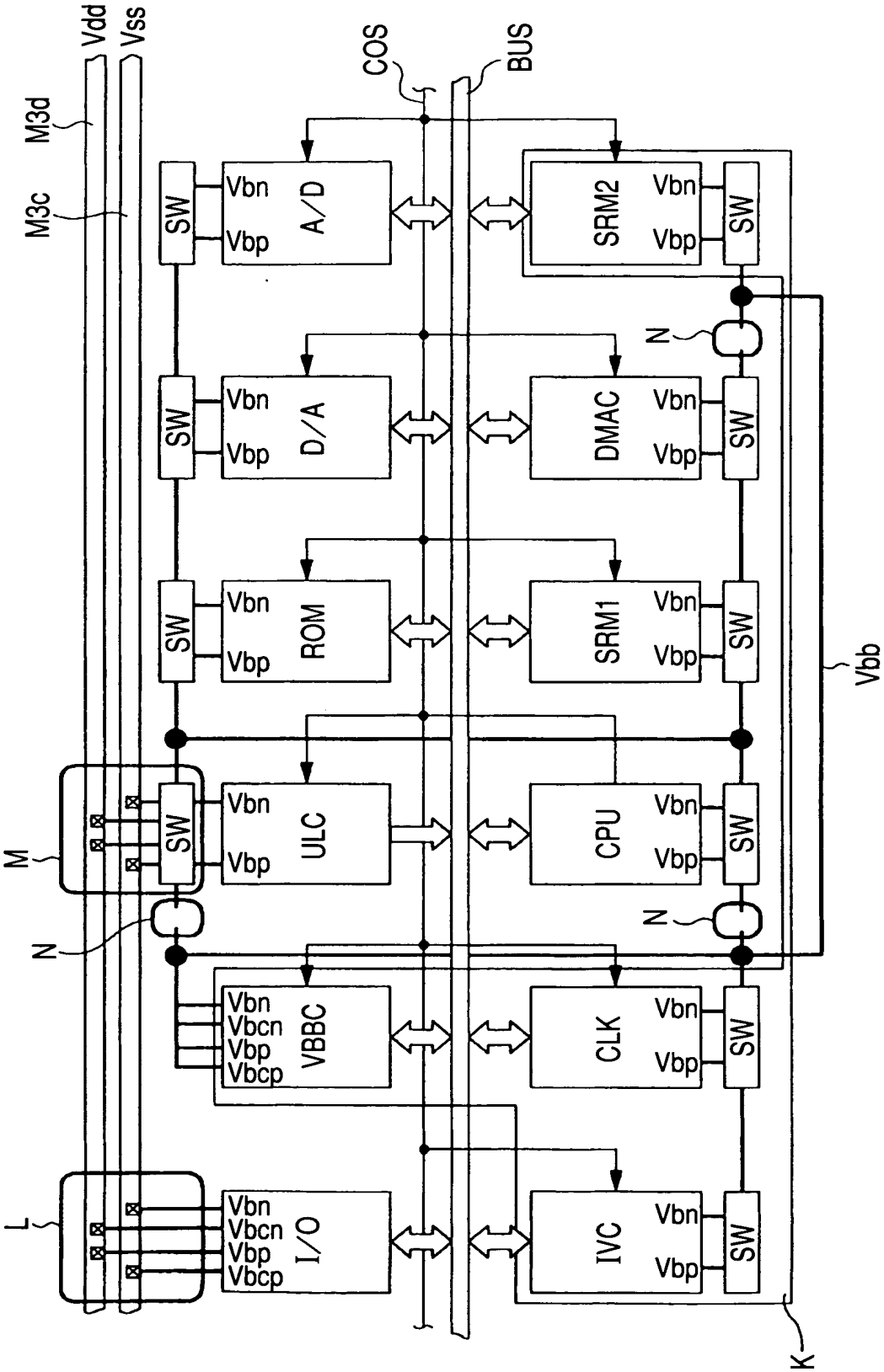

Vdd
Vss
M3d
M3c
COS
BUS
SW
Vbn
Vbp
A/D
SRM2
D/A
DMAC
ROM
SRM1
ULC
CPU
Vbcn
Vbcp
VBBC
CLK
I/O
IVC
N
M
L
K
Vbb

FIG. 17

		pMIS	
		HIGH Vth	LOW Vth
nMIS	HIGH Vth	NO NEED FOR POWER SUPPLY Vbb	NEED FOR POWER SUPPLY Vbb TO pMIS FIX Vbb POWER SUPPLY TO nMIS (Vbn, Vbcn) TO Vdd, Vss
	LOW Vth	NEED FOR POWER SUPPLY Vbb TO nMIS FIX Vbb POWER SUPPLY TO pMIS (Vbp, Vbcp) TO Vdd, Vss	NEED FOR POWER SUPPLY Vbb TO pMIS & nMIS

FIG. 18

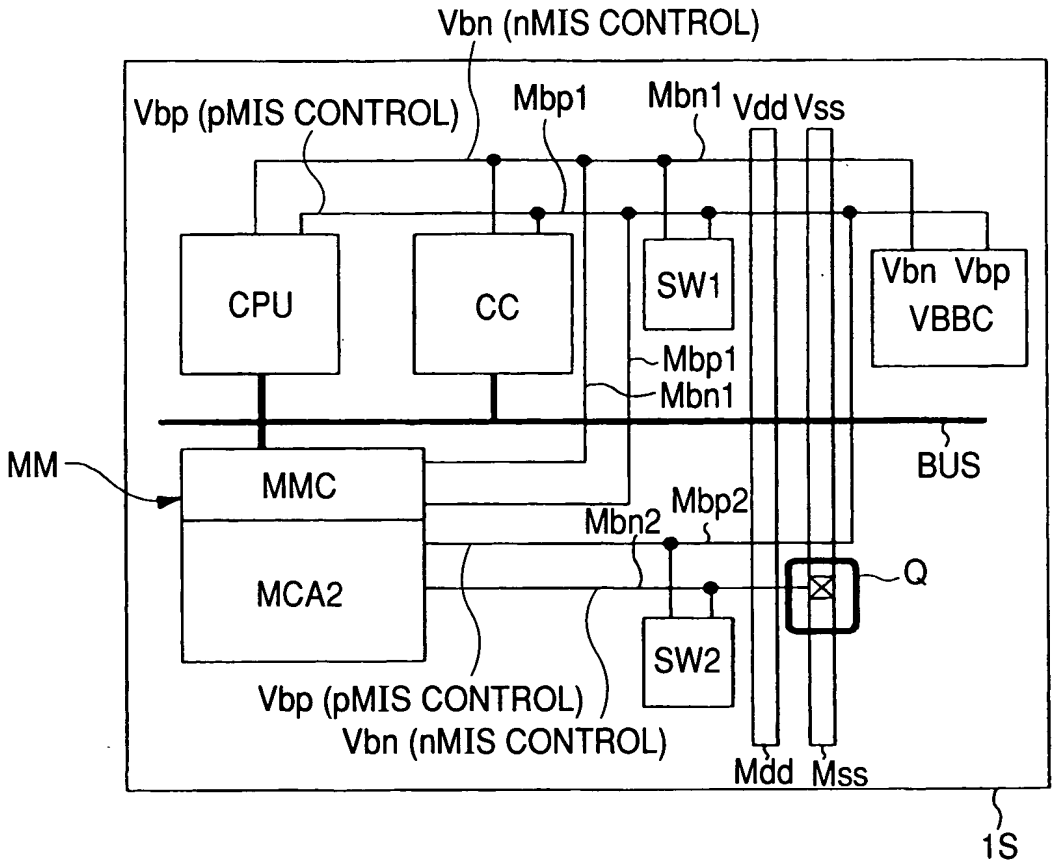

Vbn (nMIS CONTROL)
Vbp (pMIS CONTROL)
Mbp1
Mbn1
Vdd
Vss
CPU
CC
SW1
Vbn Vbp
VBBC
Mbp1
Mbn1
BUS
MM
MMC
Mbp2
Mbn2
MCA2
Q
SW2
Vbp (pMIS CONTROL)
Vbn (nMIS CONTROL)
Mdd
Mss
1S

FIG. 19

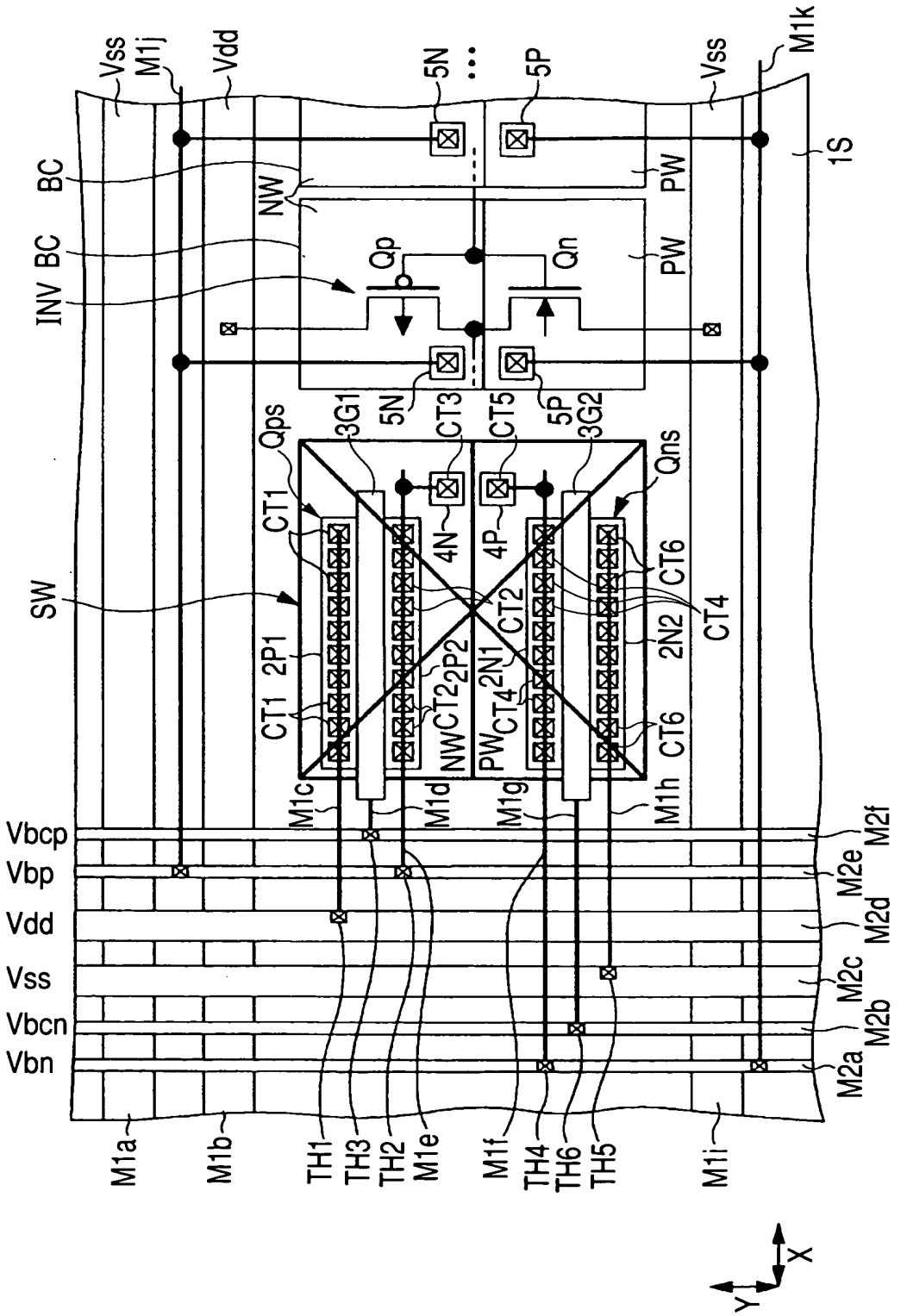

Vss
M1j
Vdd
5N
5P
Vss
M1k
1S
BC
INV BC
NW
PW
Qp
Qn
PW
3G1
5N
CT3
CT5
5P
3G2
Qps
Qns
CT1
SW
4N
4P
CT6
CT4
CT2
2P1
2P2
2N1
2N2
CT1
NW
PW
CT4
CT2
CT6
M1c
M1d
M1g
M1h
Vbcp
Vbp
Vdd
Vss
Vbcn
Vbn
M2f
M2e
M2d
M2c
M2b
M2a
M1a
M1b
TH1
TH3
TH2
M1e
M1f
TH4
TH6
TH5
M1i
X
Y

FIG. 20

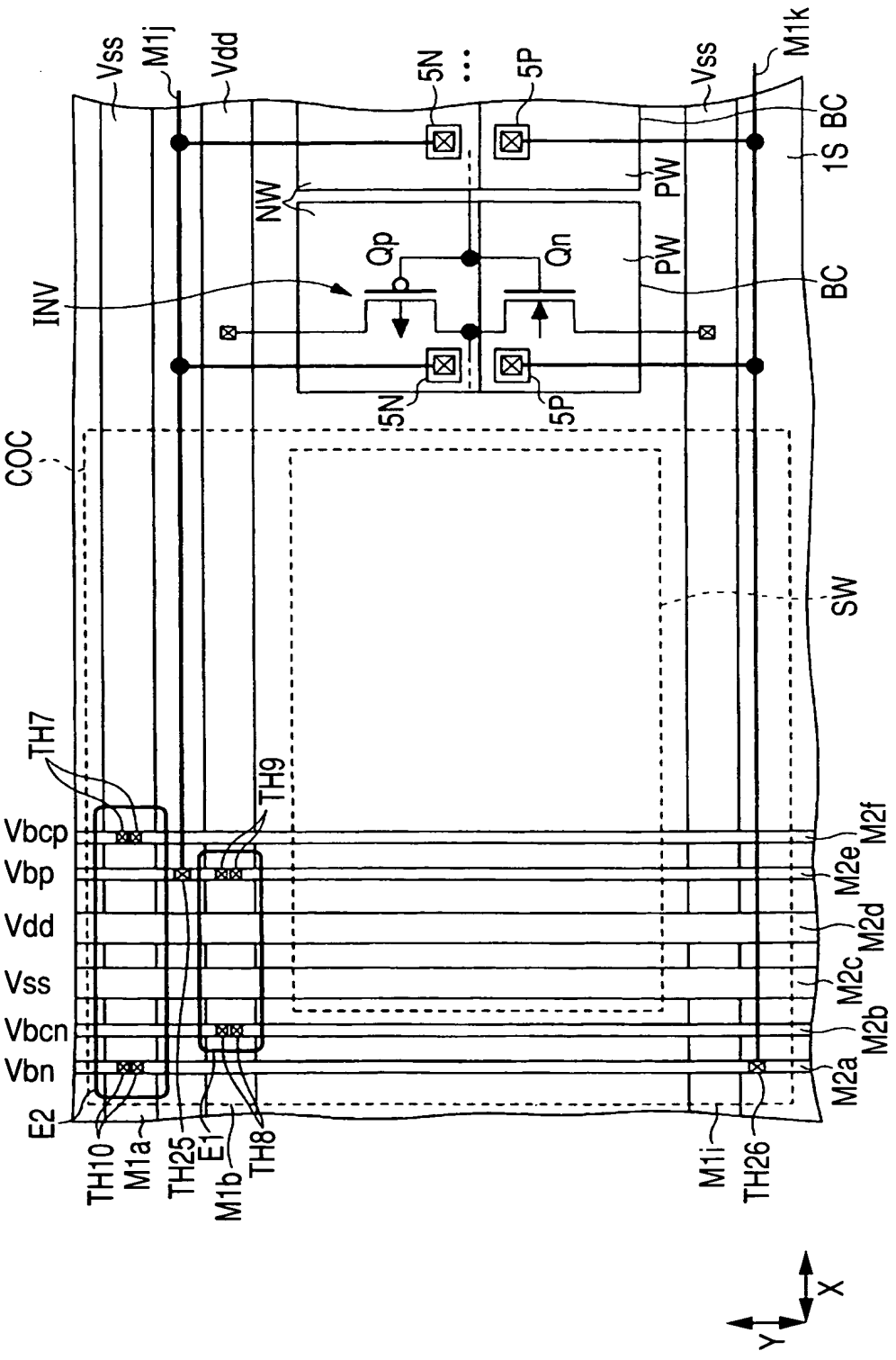
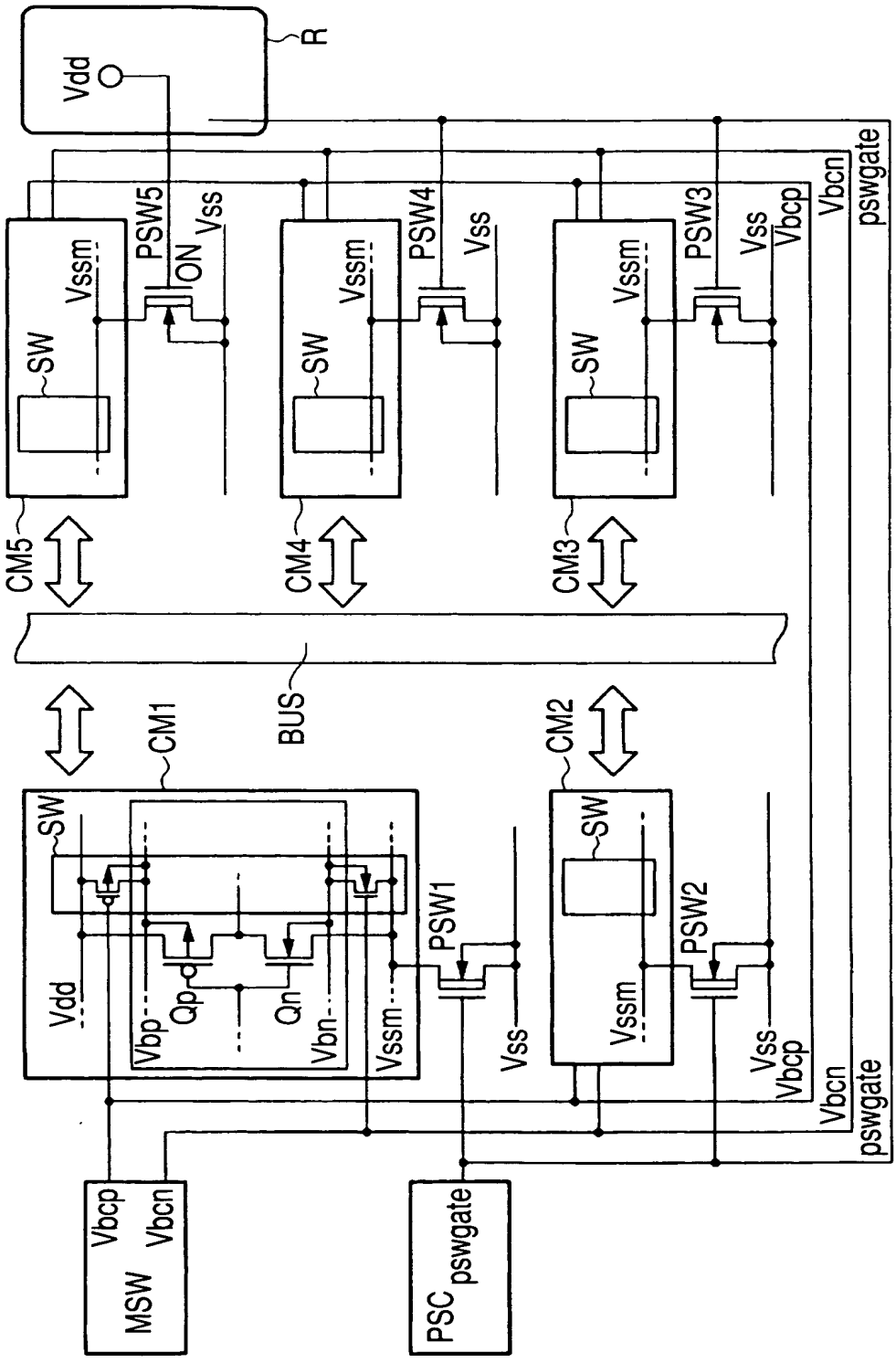

Vss
M1j
Vdd
5N
5P
Vss
M1k
1S BC
NW
PW
PW
Qp
Qn
INV
BC
5N
5P
COC
SW
TH7
TH9
Vbcp
Vbp
Vdd
Vss
Vbcn
Vbn
E2
M2f
M2e
M2d
M2c
M2b
M2a
TH10
M1a
TH25
E1
M1b
TH8
M1i
TH26
X
Y

FIG. 21


R
Vdd
PSW5
ON
Vss
Vssm
SW
PSW4
PSW3
Vbcp
Vbcn
pswgate
CM5
CM4
CM3
BUS
CM1
CM2
PSW1
PSW2
Vbp
Qp
Qn
Vbn
MSW
PSC